

FIG. 1A  
PRIOR ART

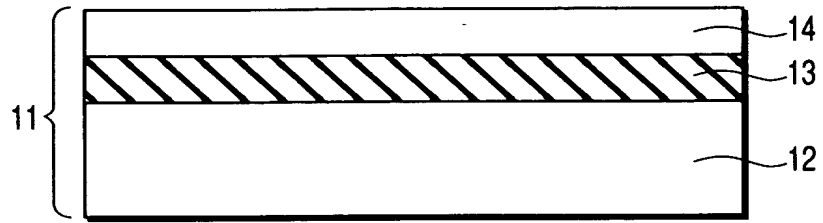


FIG. 1B  
PRIOR ART

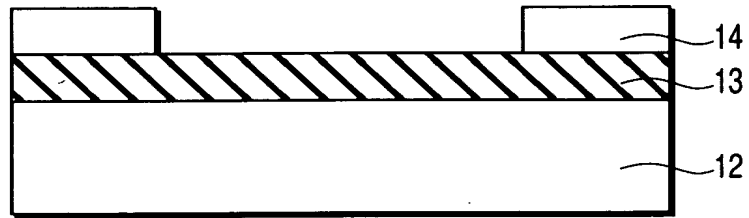


FIG. 1C  
PRIOR ART

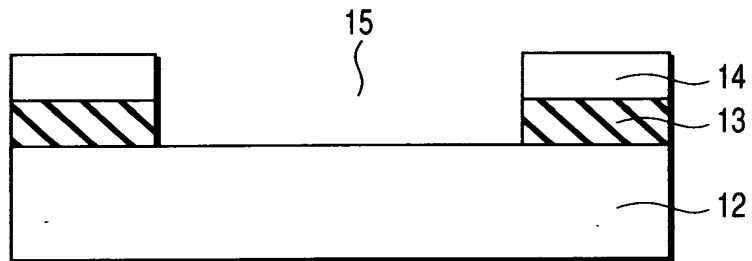


FIG. 1D  
PRIOR ART

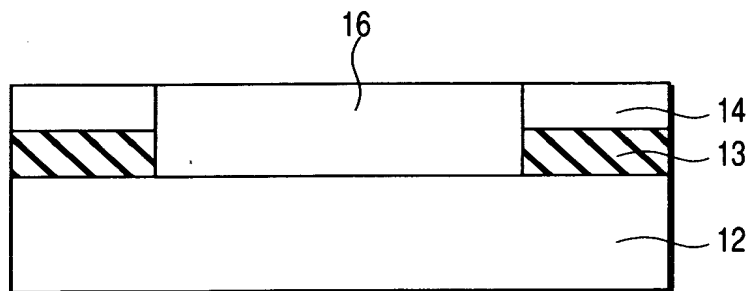
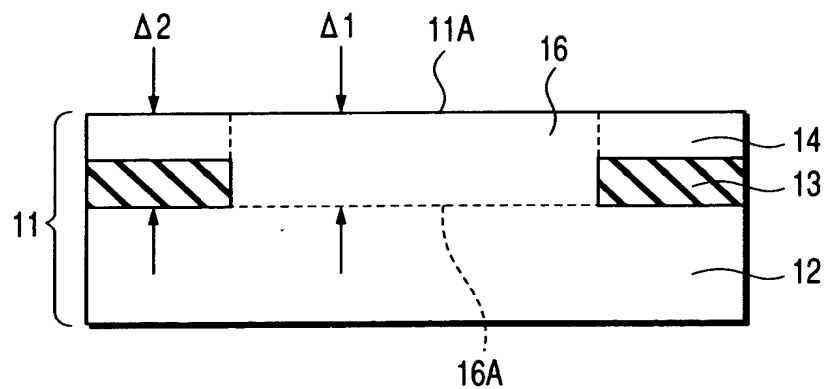


FIG. 2  
PRIOR ART



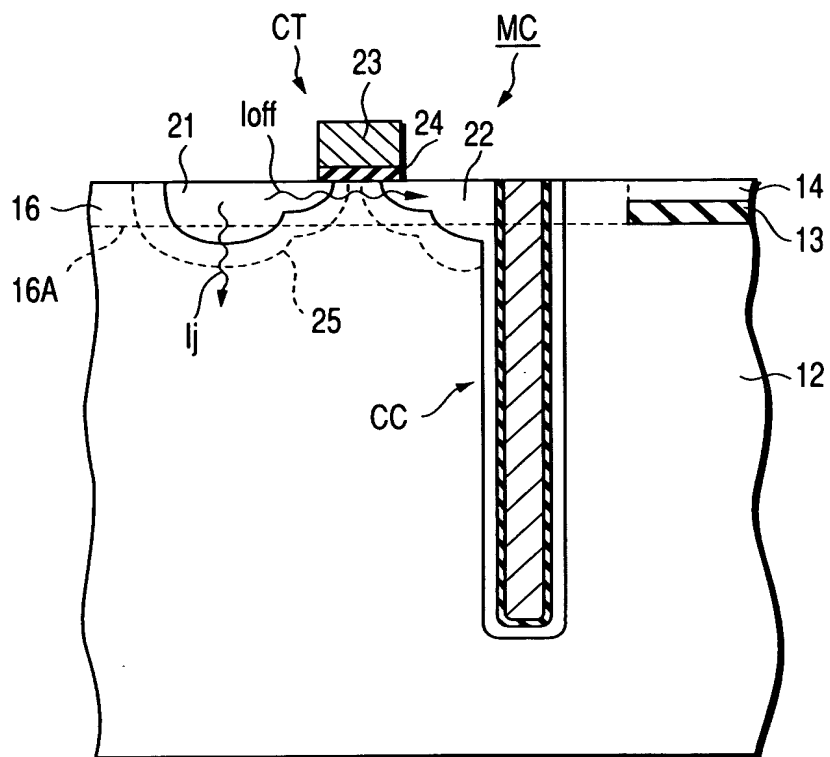


FIG. 3  
PRIOR ART

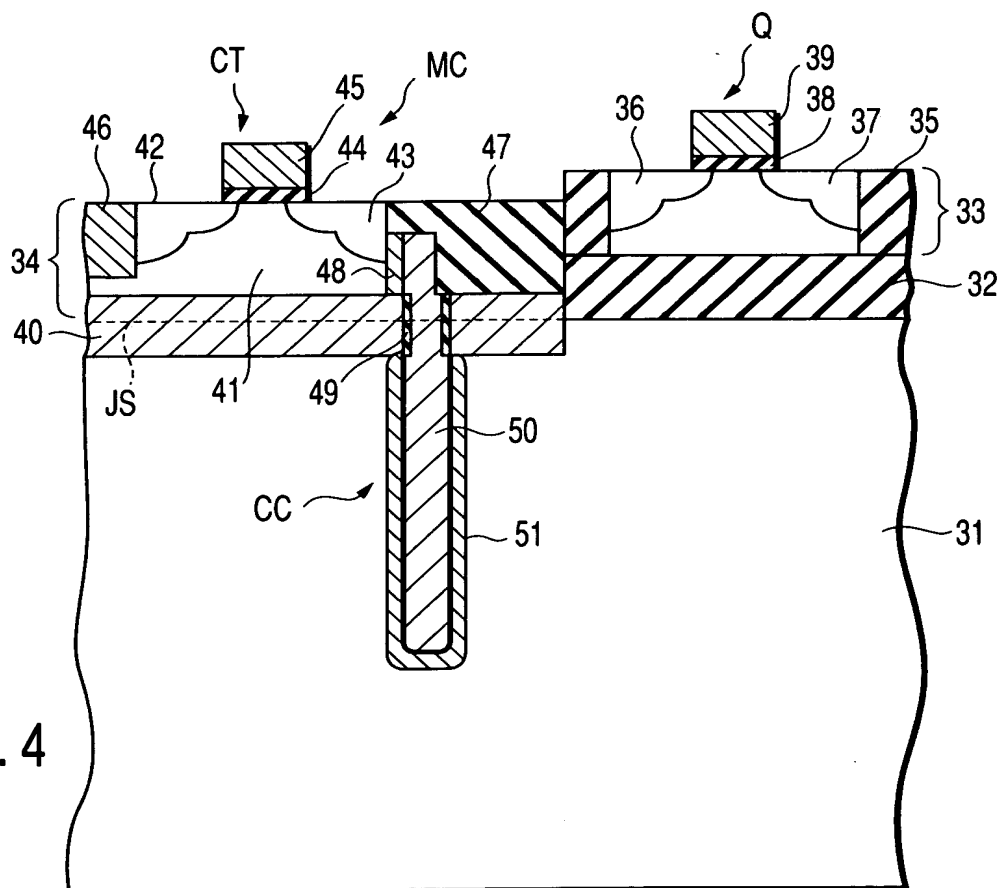


FIG. 4

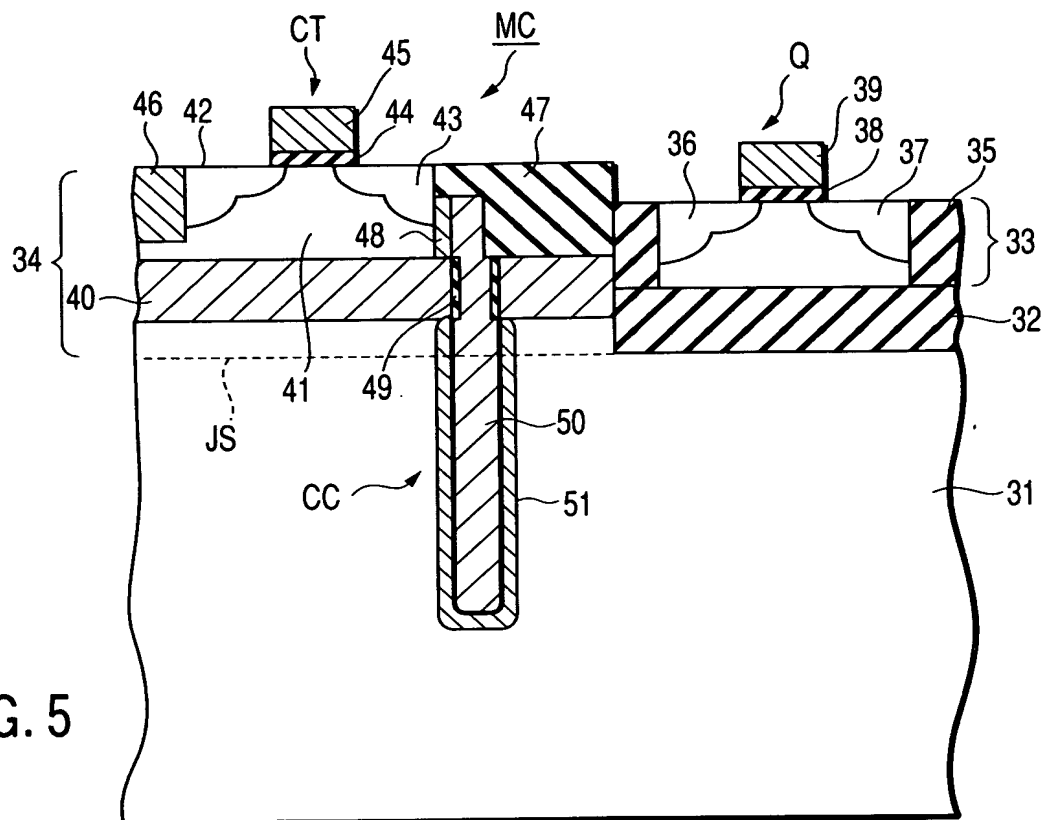


FIG. 5

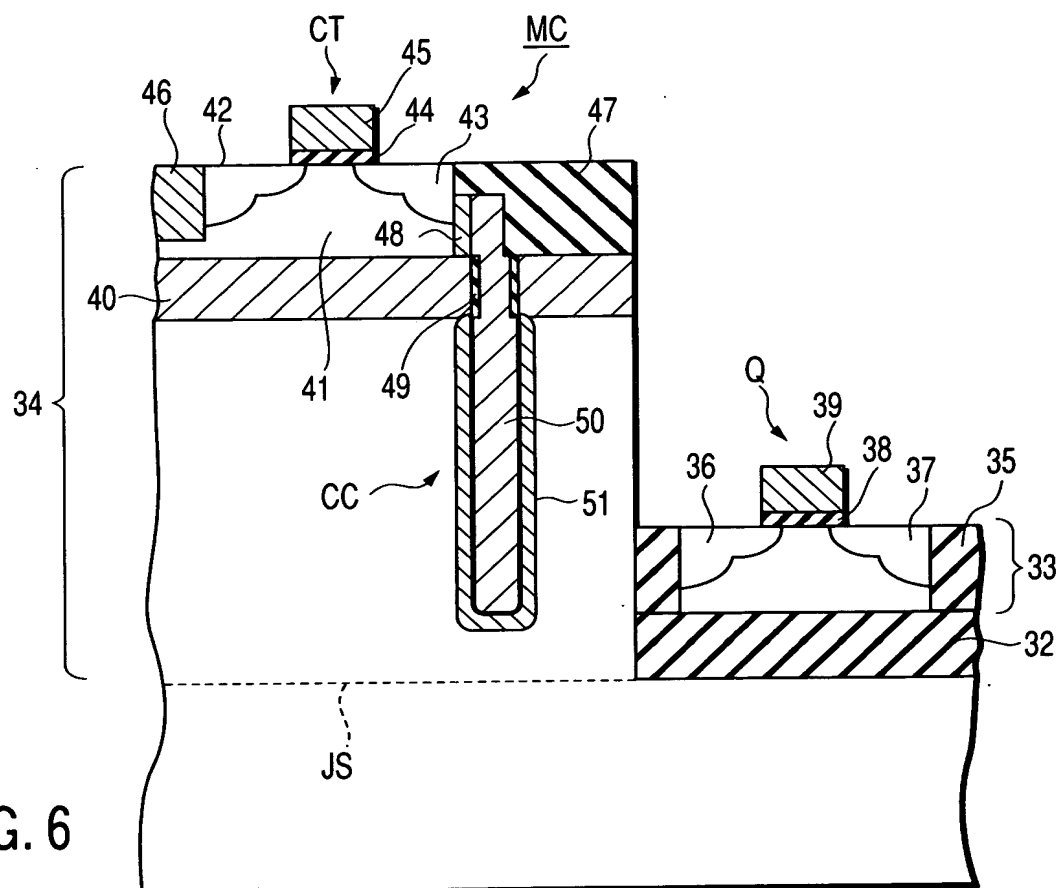


FIG. 6

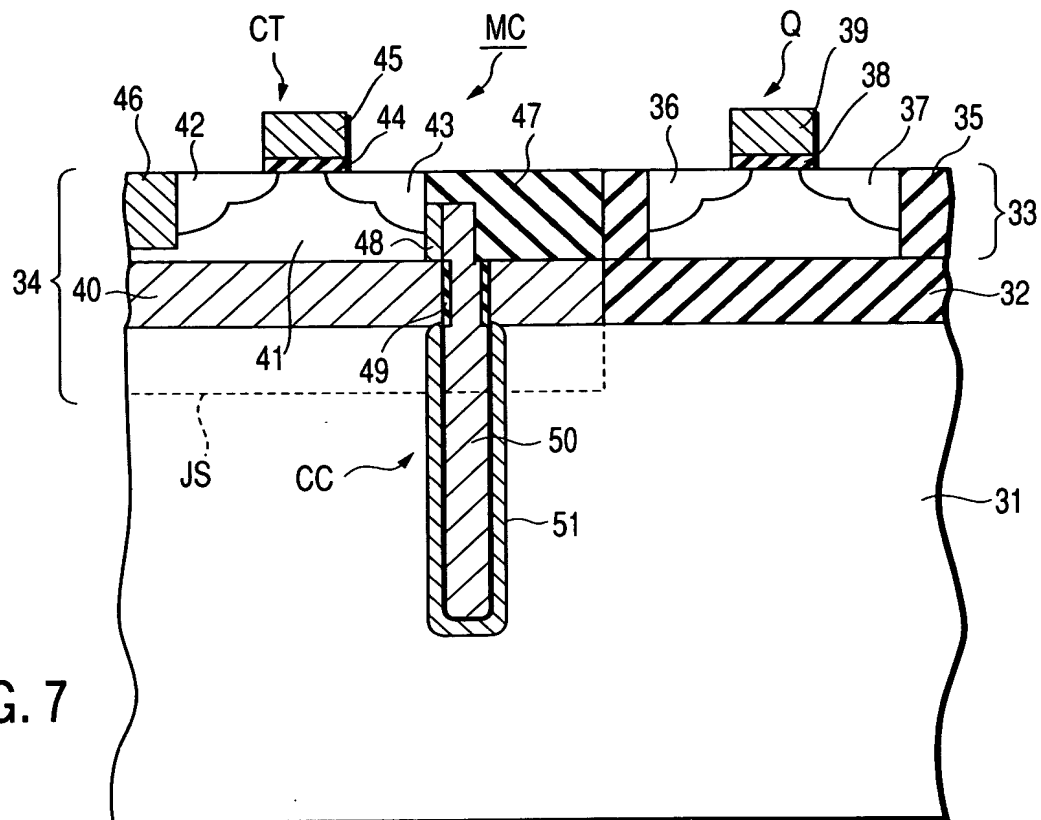


FIG. 7

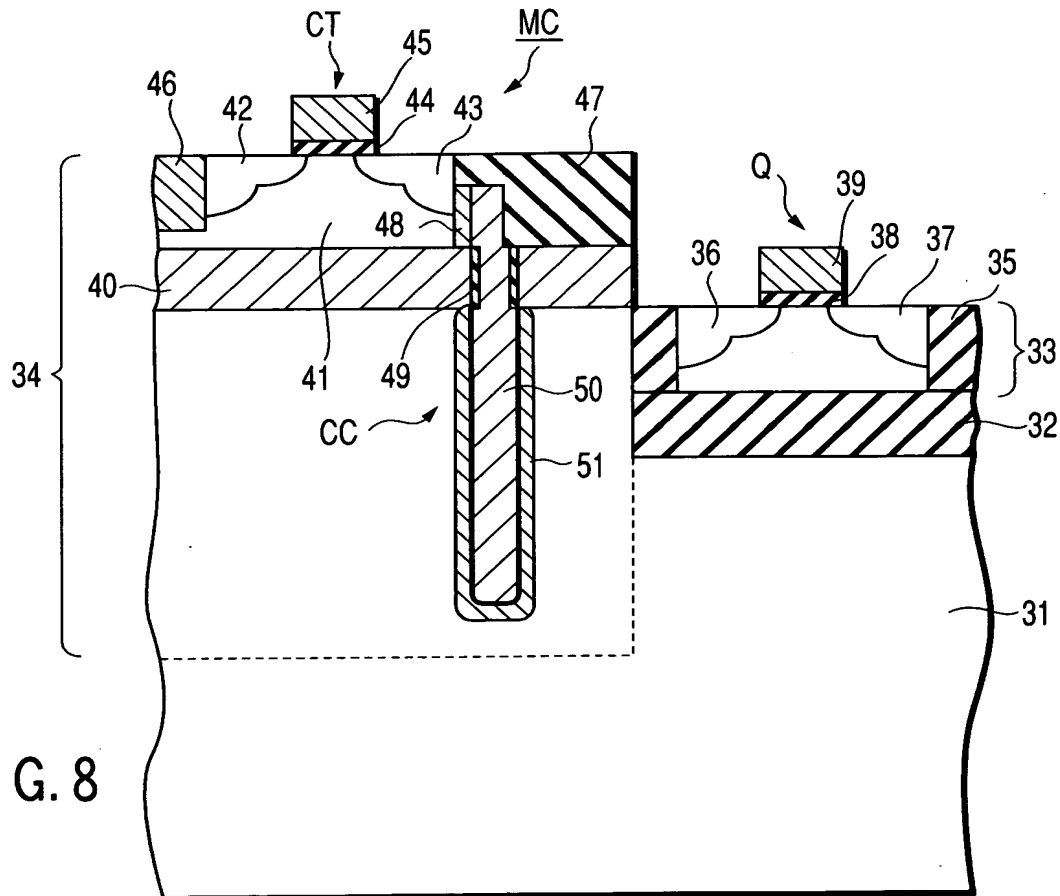


FIG. 8



FIG. 9A

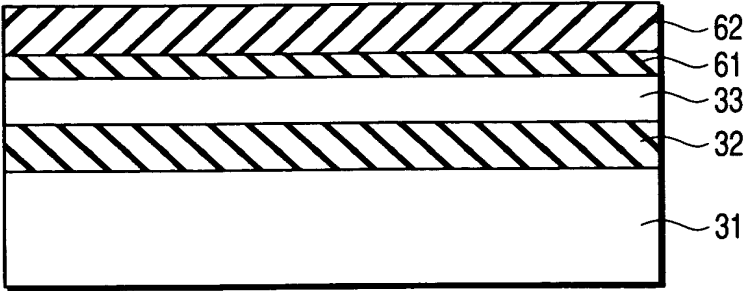


FIG. 9B

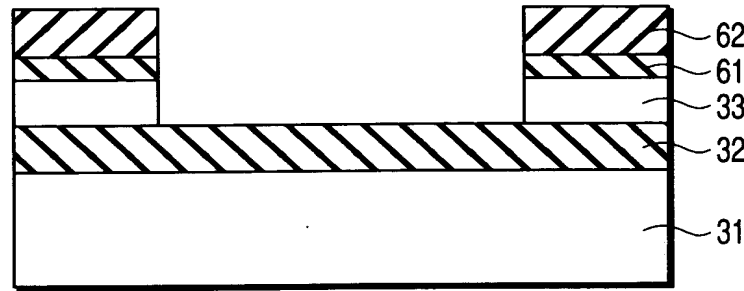


FIG. 9C

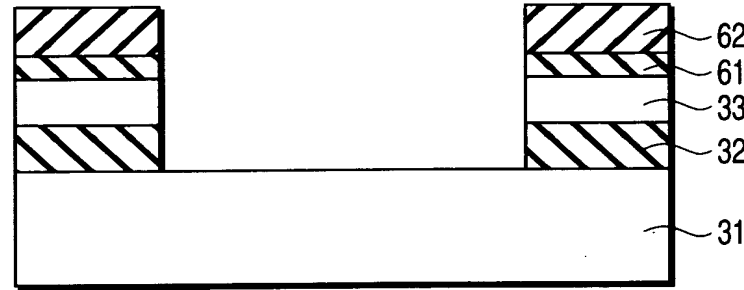


FIG. 9D

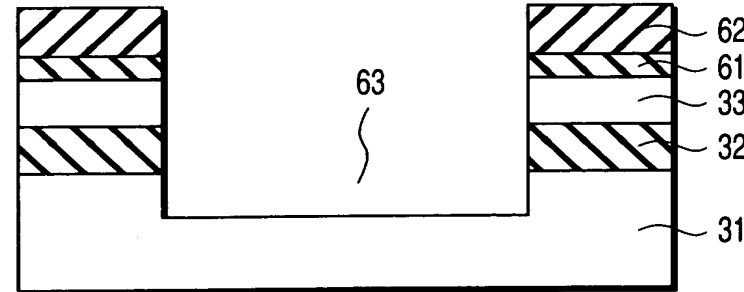


FIG. 9A

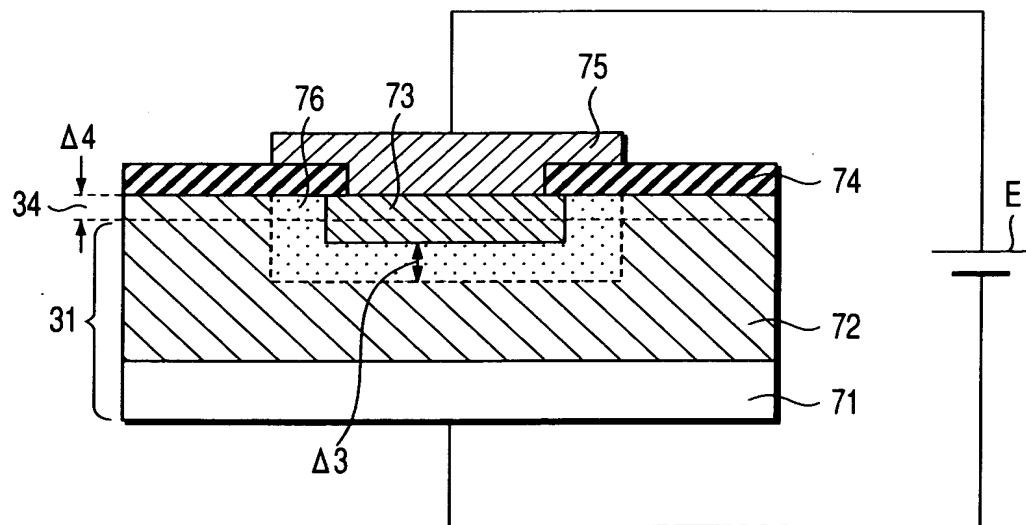


FIG. 11

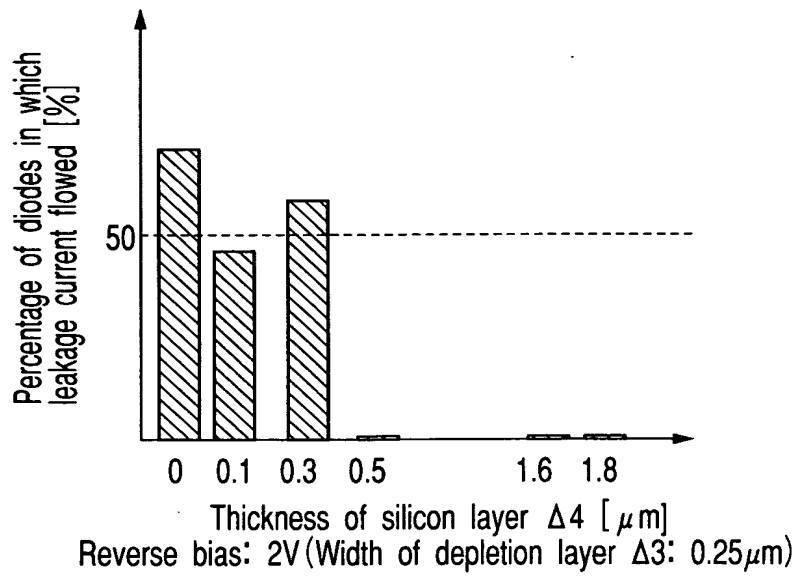


FIG. 12

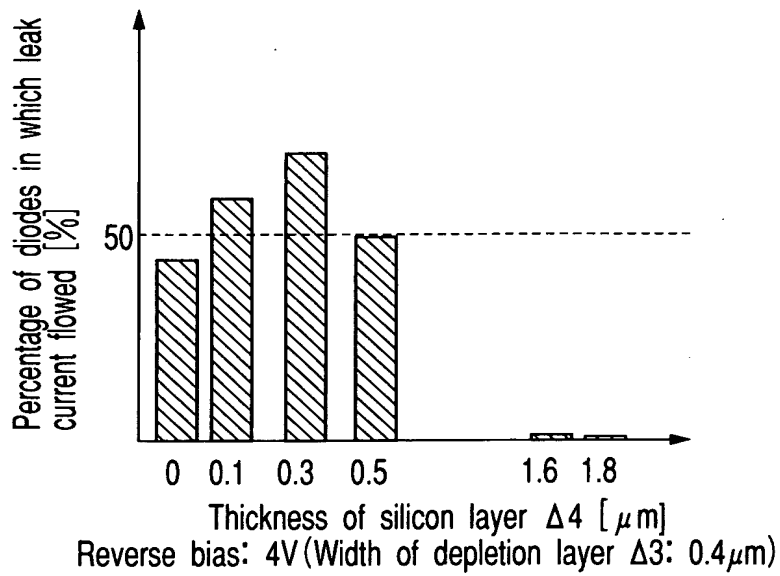


FIG. 13

- RE1: Leakage current when thickness of silicon layer is set at 0, 0.1, 0.3  $\mu\text{m}$   
RE2: Leakage current when thickness of silicon layer is set at 0.5  $\mu\text{m}$   
RE3: Leakage current in this embodiment (when thickness of silicon layer is set at 1.6, 1.8  $\mu\text{m}$ )

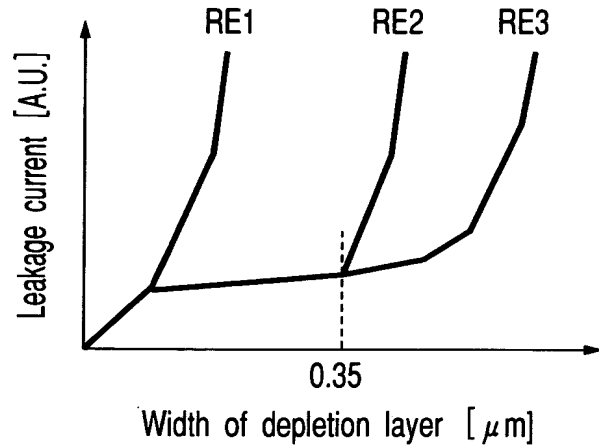


FIG. 14

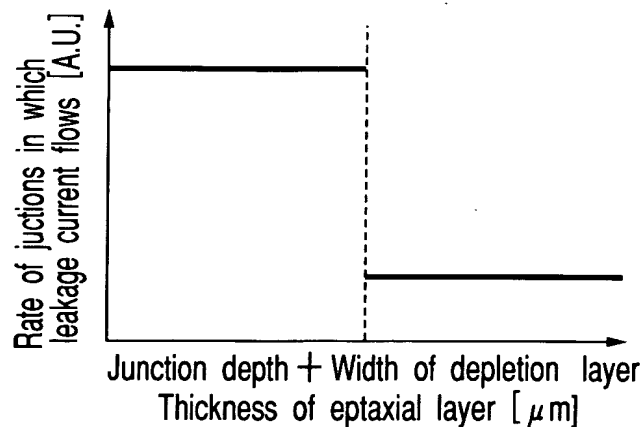


FIG. 15



FIG. 16A

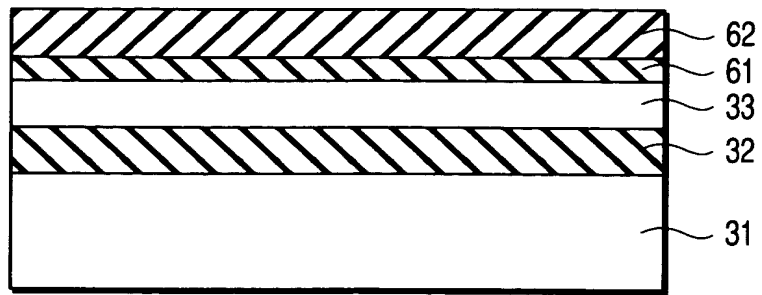


FIG. 16B

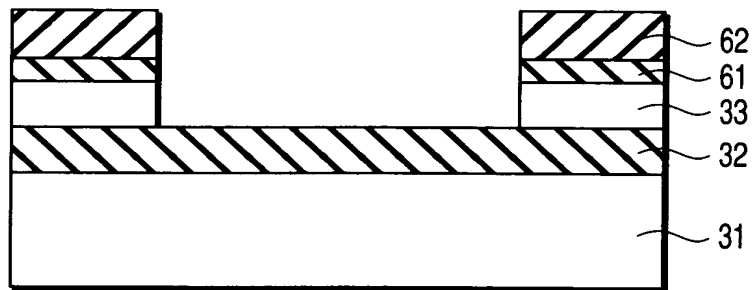


FIG. 16C

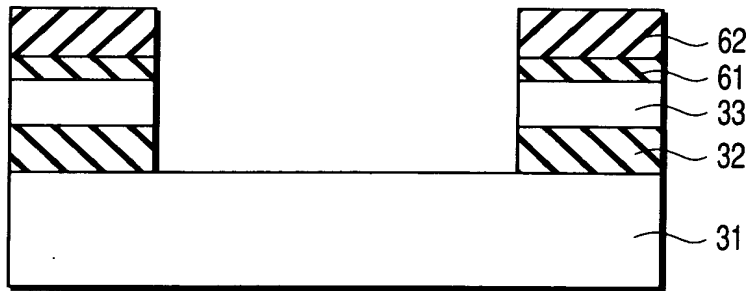


FIG. 16D

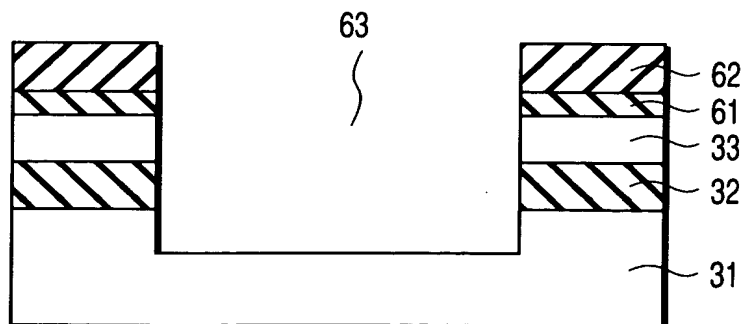


FIG. 16E

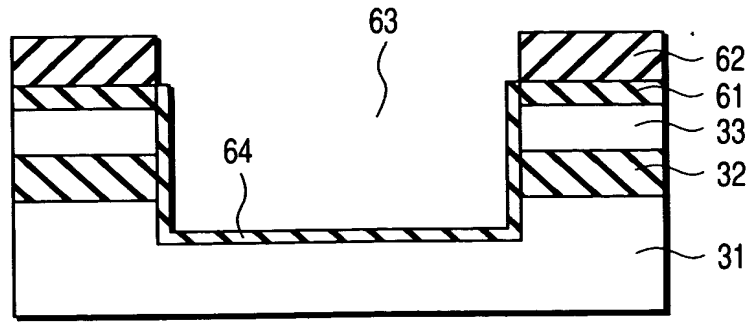


FIG. 16F

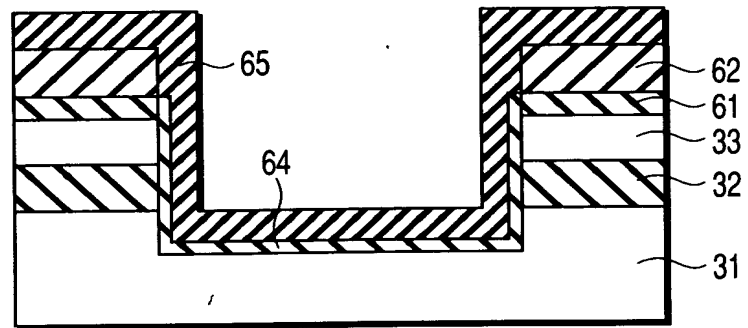


FIG. 16G

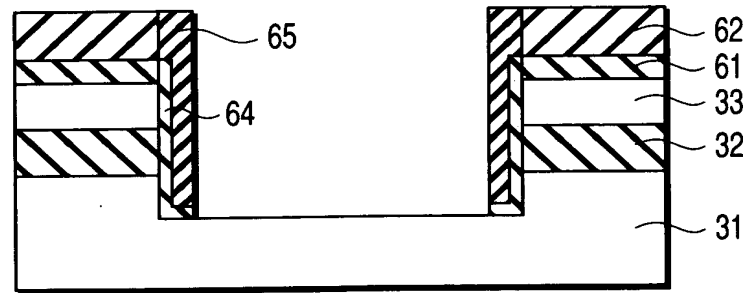
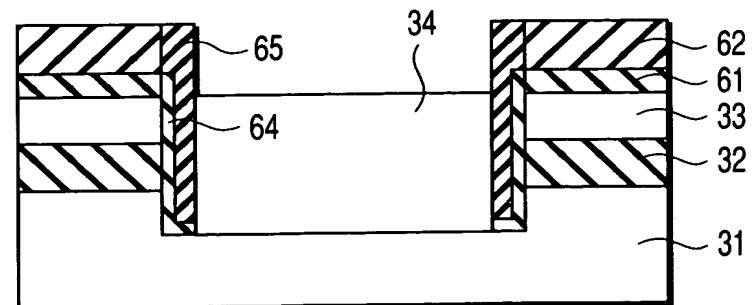


FIG. 16H



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FIG. 17

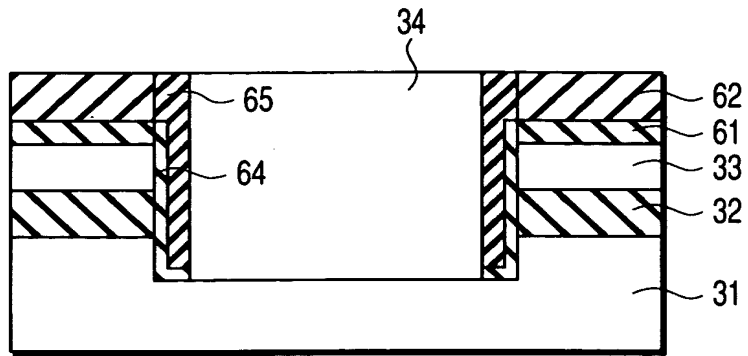


FIG. 18A

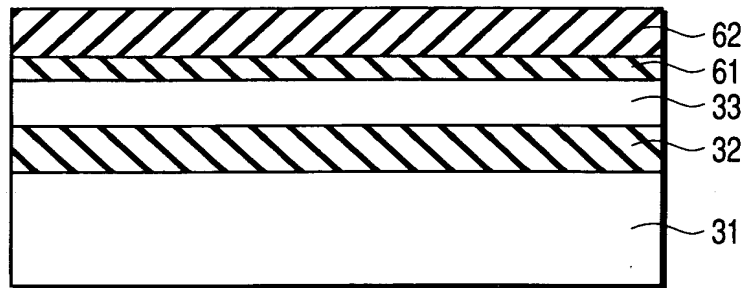


FIG. 18B

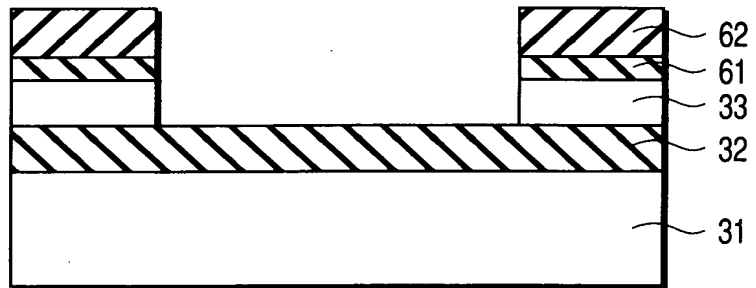


FIG. 18C

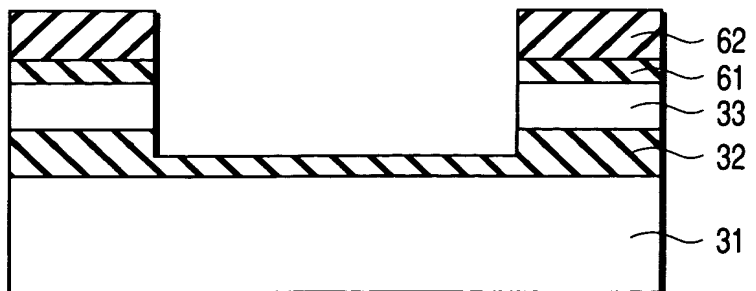


FIG. 17

FIG. 18D

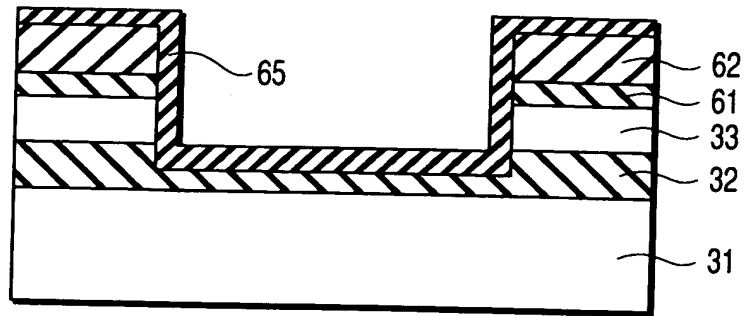


FIG. 18E

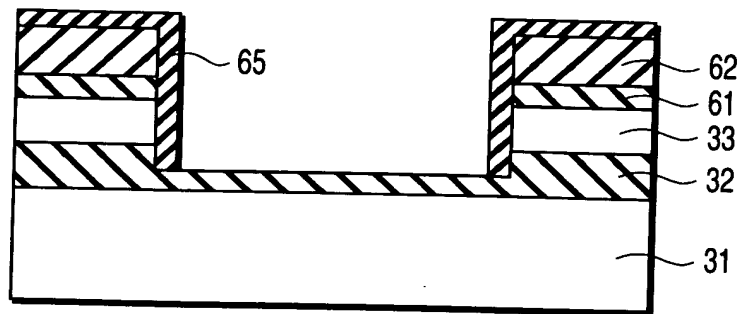


FIG. 18F

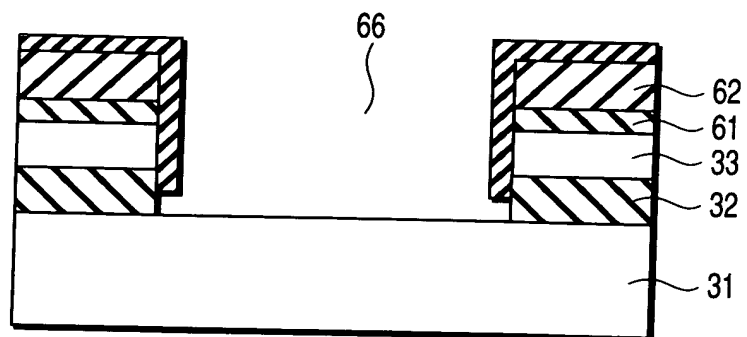


FIG. 18G

